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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Hirofumi HARADA

Serial No. 09/872,798

: Group Art Unit - 2814

Filed: June 1, 2001

: Examiner - Thao S. Le

For: VERTICAL MOS TRANSISTOR

AND A METHOD OF

MANUFACTURING THE SAME

: Docket No. S004-4310

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COMMISSIONER OF PATENTS AND TRADEMARKS Washington, DC 20231

RECEIVED

MAR 1 3 2002

RESPONSE

Technology Center 2100

S I R:

In response to the Office Action dated February 6, 2002, applicant amends his application as follows:

## ELECTION OF INVENTION:

Applicant provisionally elects, with traverse, the invention characterized by the Examiner as Group I drawn to semiconductor devices and submits that claims 1-5 are readable on the elected invention.

MAILING CERTIFICATE ON REVERSE SIDE OF LAST PAGE